a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit disposed on the semiconductor substrate;

wherein the memory cell has a multi-layer of a conductive layer, an insulating layer and plural semiconductor layers containing impurities of different conduction type, and a potential can be applied to the insulating layer that enables the movement of carriers by way of the multi-layer.

8. (Amended) A semiconductor memory device as defined in claim 4, wherein an impurity concentration of the layer present in contact with the surface of the semiconductor substrate among the plural semiconductor layers containing impurities for forming the memory cell is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.

30. (Amended) A semiconductor memory device as defined in claim 1, wherein at least a portion of a memory device is disposed in the semiconductor substrate and a memory capacity is 256 Mbits or more.

Please add the following claims:

32. (New) A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit disposed on the semiconductor substrate;

wherein the memory cell has a multi-layer of a conductive layer, an insulating layer and plural semiconductor layers containing impurities, and a current that flows when a potential is applied to the insulating layer capable of moving carriers by way of the multi-layer has a hysteresis characteristic relative to the applied voltage.

33. (New) A semiconductor memory device as defined in claim 5, wherein an impurity concentration of the layer present in contact with the surface of the semiconductor substrate among the plural semiconductor layers containing impurities for forming the memory cell is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.

34. (New) A semiconductor memory device as defined in claim 6, wherein an impurity concentration of the layer present in contact with the surface of the semiconductor substrate among the plural semiconductor layers containing impurities for forming the memory cell is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.

35. (New) A semiconductor memory device as defined in claim 7, wherein an impurity concentration of the layer present in contact with the surface of the semiconductor substrate among the plural semiconductor layers containing impurities for forming the memory cell is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.

REMARKS

Claims 1 and 30 have been amended and Claim 32 has been added to conform with the amendments submitted during the international stage.

Claim 8 has been amended to avoid the surcharge for multiple dependent claims. Claims 33-35 correspond to the dependencies eliminated from 8.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by